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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,957	12/23/2003	Gordon Keith Grimes	03-0376	9374

24319 7590 02/16/2006

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EXAMINER	
WALLING, MEAGAN S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EJL

Office Action Summary	Application No.	Applicant(s)	
	10/743,957	GRIMES ET AL.	
	Examiner	Art Unit	
	Meagan S. Walling	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-13,16-18 and 20* is/are rejected.

7)☒ Claim(s) *4,6,7,14,15 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3, 8-13, 16-18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Gates et al. (US 6,516,366).

Regarding claim 1, Gates et al. teaches initiating a test mode within a host adapter board (column 11, lines 23-26); generating a clock signal for the host adapter board Fig. 2A, Ref. CLK40); generating PCI signals (250) within the host adapter board (240) wherein the step of generating uses an I/O controller (221) of the host adapter board; electronically selecting one or more PCI signal lines of the host adapter board wherein the step of selecting uses an I/O controller of the host adapter board (column 41, lines 41-42); and assessing timing of the one or more PCI signals from the PCI signal lines (see Table 14A).

Regarding claim 2, Gates et al. teaches utilizing addresses within memory of the host adapter board to select the one or more PCI signal lines (column 3, lines 59-63).

Regarding claim 3, Gates et al. teaches storing addresses within the memory (column 3, line 36).

Regarding claim 8, Gates et al. teaches utilizing a logic analyzer (column 3, lines 59-63).

Regarding claim 9, Gates et al. teaches utilizing a signal generated connected with the host adapter board (column 2, line 44-47).

Regarding claim 10, Gates et al. teaches assessing one or both of slew rate and clock-to-signal valid of the PCI signals (column 41, lines 31-34).

Regarding claim 11, Gates et al. teaches a host adapter board (240) responsive to a test mode initialization to generate PCI signals within the host adapter board (column 11, lines 23-26), the host adapter board having internal memory (224) for storing addresses for PCI signal lines of the host adapter board, the host adapter board adapted to receive an external clock signal (CLK40) and being configured to select one or more of the PCI signal lines, based on the addresses, for output from host adapter board (column 3, lines 59-63 and column 41, lines 41-42); and a PCI test controller for assessing PCI signals from the output and relative to the clock signal (see Table14A).

Regarding claim 12, Gates et al. teaches assessing one or both of clock-to-signal valid and slew rate from the output (column 41, lines 31-34).

Regarding claim 13, Gates et al. teaches an I/O controller (221) that includes the internal memory (224), the I/O controller operable to facilitate communications between the host adapter board and an electronic device connected to the host adapter board (Fig. 2A, Ref. 243 and 284).

Regarding claim 16, Gates et al. teaches a generator for generating the PCI signals (column 2, line 66 – column 3, line 3).

Regarding claim 17, Gates et al. teaches means for initiating a test mode within a host adapter board (column 11, lines 23-26); means for generating a clock signal for the host adapter board (CLK40 and column 2, lines 44-47); means for generating PCI signals (250) within the

host adapter board (240) wherein the means for generating includes an I/O controller (221) of the host adapter board; means for electronically selecting one or more PCI signal lines of the host adapter board wherein the means for electronically selecting includes an I/O controller of the host adapter board (column 41, lines 41-42); and means for assessing timing of the one or more PCI signals from the PCI signal lines (see Table 14A).

Regarding claim 18, Gates et al. teaches that the I/O controller further comprises internal memory (224) for storing addresses of the one or more PCI signals (column 3, line 36).

Regarding claim 20, Gates et al. teaches determining one or both of clock-to-signal valid and slew rate for the one or more PCI signal lines (column 41, lines 31-34).

Allowable Subject Matter

2. Claims 4, 6, 7, 14, 15, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the indication of allowability of claim 4 is the inclusion of the limitation that storing comprises loading addresses into I/O controller memory. It is this limitation in the claimed combination that has not been found, taught, or suggested in the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 6 is the inclusion of the limitation of utilizing a jumper connected between the host adapter board and an external

electronic device. It is this limitation in the claimed combination that has not been found, taught, or suggested in the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 7 is the inclusion of the limitation of cycling through addresses within memory of the host adapter board. It is this limitation in the claimed combination that has not been found, taught, or suggested in the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 14 is the inclusion of the limitation of the controller having a switch for toggling the one or more PCI signal lines based upon the addresses. It is this limitation in the claimed combination that has not been found, taught, or suggested in the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 14 is the inclusion of the limitation of the controller having a switch for toggling the one or more PCI signal lines based upon the addresses. It is this limitation in the claimed combination that has not been found, taught, or suggested in the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 19 is the inclusion of means for cycling through the addresses such that, over time, the means for assessing assesses different PCI signals of the host adapter board. It is this limitation in the claimed combination that has not been found, taught, or suggested in the prior art that makes these claims allowable.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S. Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw

BRYAN BUI
PRIMARY EXAMINER